

IP175C MII Application Note

Register setting and pin connection

Application Note

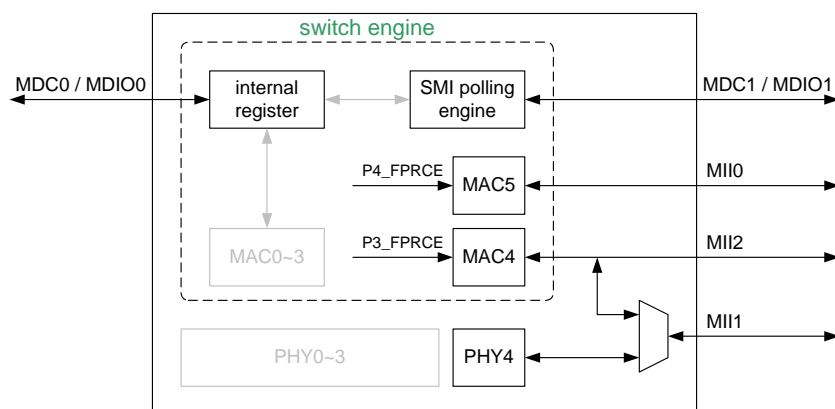
Rev. 0.10

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1. Summary of MII applications



I/F	mode	Int	ext	p4ext	mii1_dis	mii2_en	p4mii_sni	rmii_en	mii0_mac_mod	mii1_phy_mode	mii2_mac_mod
MII0											
MII	PHY mode	MAC5	MAC	1	X	X	0	0	0	X	X
MII	MAC mode	MAC5	PHY	1	X	X	0	0	1	X	X
RMII	MAC	MAC5	Note1	1	X	X	0	1	X	X	X
SNI	PHY mode	MAC5	MAC	1	X	X	1	0	0	X	X
SNI	MAC mode	MAC5	PHY	1	X	X	1	0	1	X	X
MII1											
MII	PHY mode	PHY4	MAC	1	0	X	X	X	X	1	X
MII	MAC mode	MAC4	PHY	1	0	0	X	X	X	0	X
RMII	PHY mode	PHY4	MAC	1	0	X	X	1	X	1	X
RMII	MAC mode	MAC4	PHY	1	0	0	X	1	X	0	X
MII2											
MII	PHY mode	MAC4	MAC	1	X	1	X	X	X	X	0
MII	MAC mode	MAC4	PHY	1	X	1	X	X	X	X	1
RMII	MAC	MAC4	Note1	1	X	1	X	1	X	X	X

Note1: The port can be connected to an external PHY or MAC device.

Note2:

I/F: the kind of interface

Mode: the port looks like a MAC or a PHY

Int: the internal port to which the MII port is connected

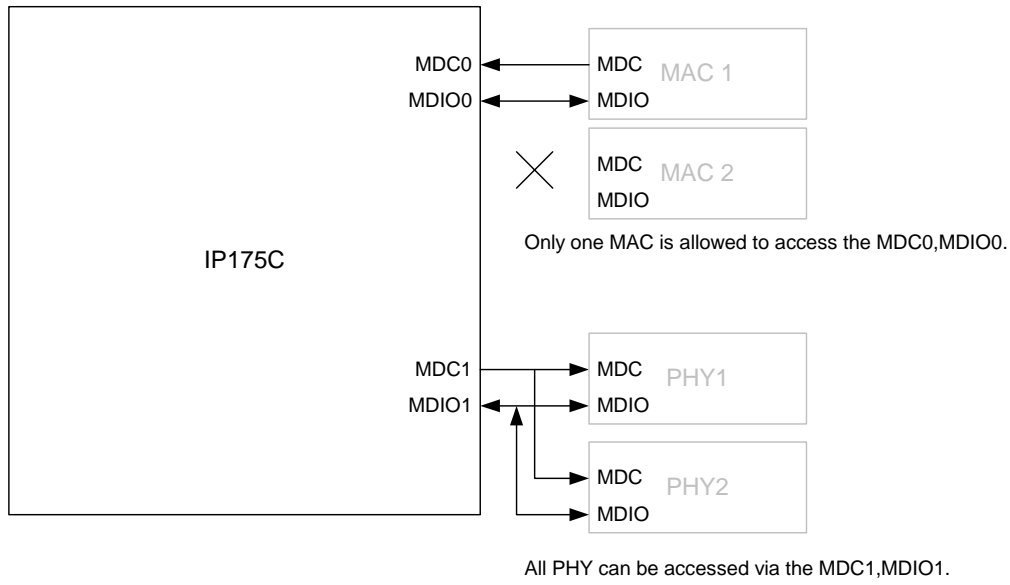
Ext: the external device to which the MII port is connected

MAC4: the port 4 of switch engine, which consists of port 0~5

MAC5: the port 5 of switch engine, which consists of port 0~5

PHY4: the port 4 of PHY, which consists of port 0~4

2. The application of MDC, MDIO¹

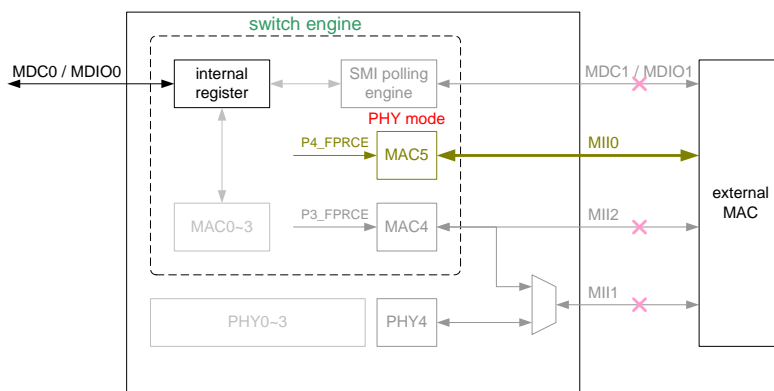


¹ P4EXT = 1

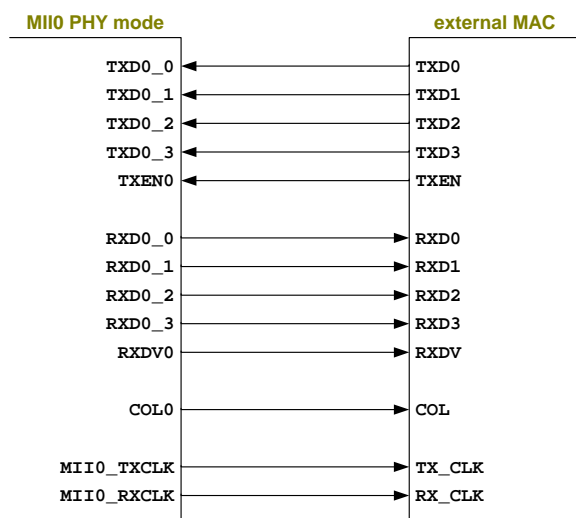
3. MII connection

3.1. MII0 port

3.1.1. MII0 PHY mode



● Pin connection



● Pin setting

Pin name	setting
P4EXT	1 ²
RMII_EN	0 ³
MII0_MAC_MOD	0
P4MII_SNI	0

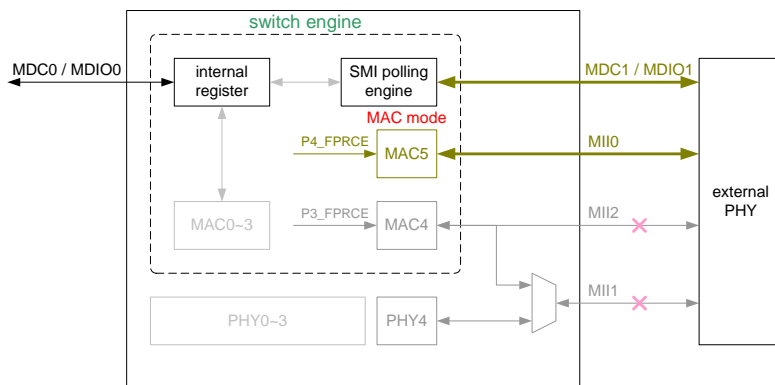
● Register setting

PHY Add.	Register #	Bit	Description	Value
31	5	15	P4EXT	1
31	5	11	MII0_MAC_MODE_EN	0
31	5	10	RMII_EN	0

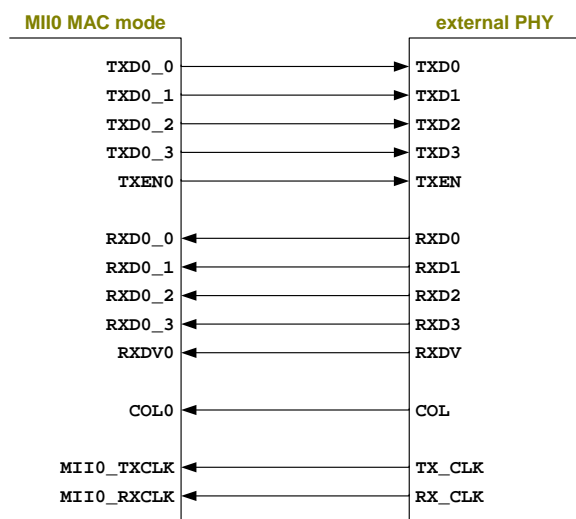
² Pull high

³ Pull low

3.1.2. MII0 MAC mode



● Pin connection



● Pin setting

Pin name	setting
P4EXT	1
RMII_EN	0
MII0_MAC_MOD	1
P4MII_SNI	0

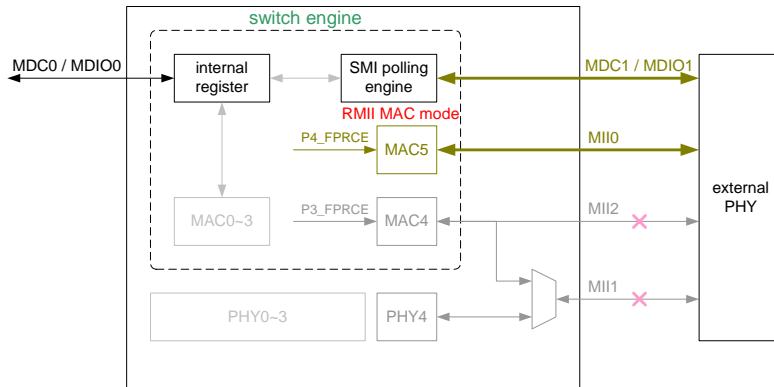
● Register setting

PHY Add.	Register #	Bit	Description	Value
31	3	12:8	Capability of external PHY on MII0	UD ⁴
31	3	4:0	MII0_MAC_PHY_ADDR ⁵	UD
31	5	15	P4EXT	1
31	5	11	MII0_MAC_MODE_EN	0
31	5	10	RMII_EN	0

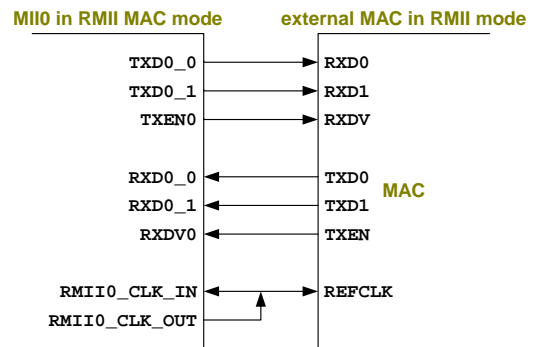
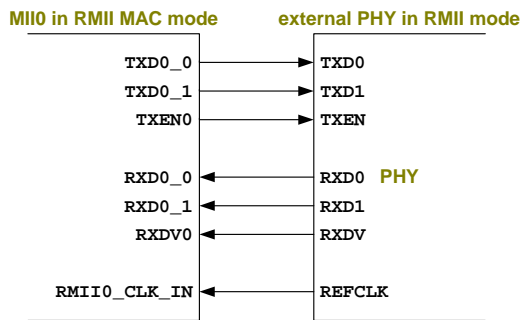
⁴ User defined value. The SMI logic will use this user defined value to access the external PHY register after reset.

⁵ External PHY address of MII0

3.1.3. MII0 RMII MAC mode



● Pin connection⁶



● Pin setting

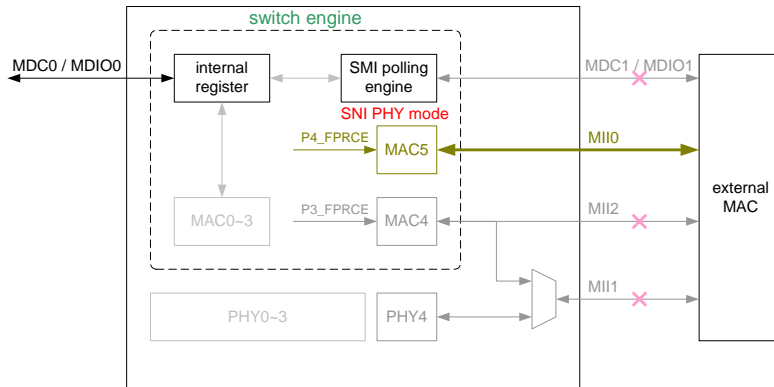
Pin name	setting
P4EXT	1
RMII_EN	1
P4MII_SNI	0

● Register setting

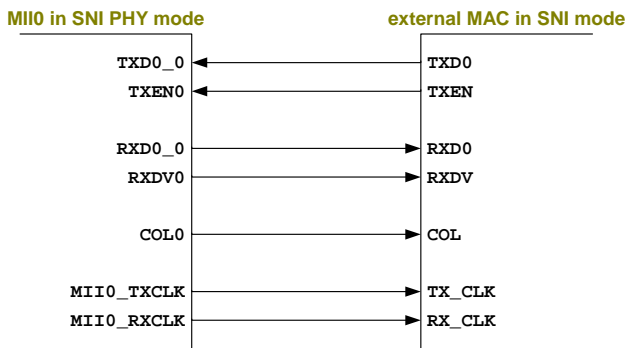
PHY Add.	Register #	Bit	Description	Value
31	3	12:8	Capability of external PHY on MII0	UD
31	3	4:0	MII0_MAC_PHY_ADDR	UD
31	5	15	P4EXT	1
31	5	10	RMII_EN	1

⁶ Under this mode, this port can be connected to an external PHY or MAC device.

3.1.4. MII0 SNI PHY mode



● Pin connection



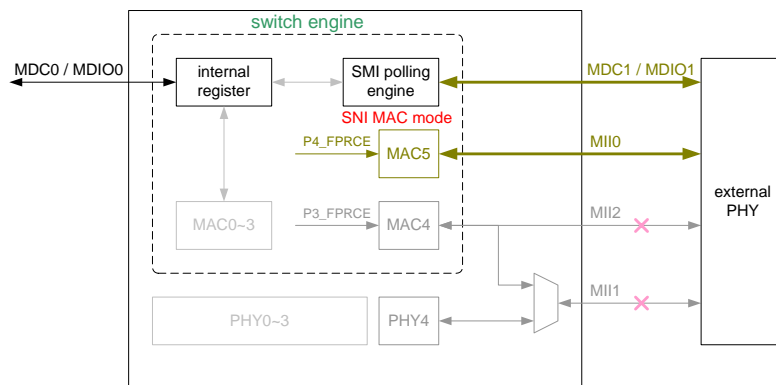
● Pin setting

Pin name	setting
P4EXT	1
RMII_EN	0
MII0_MAC_MOD	0
P4MII_SNI	1

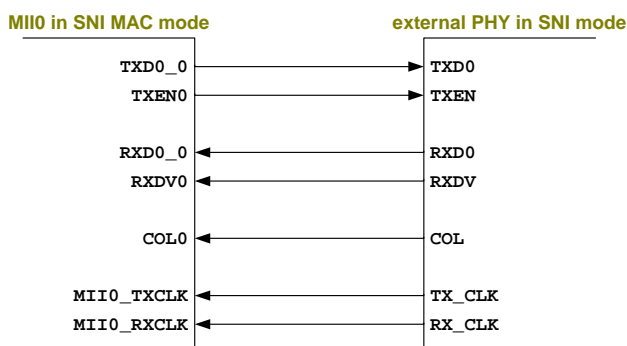
● Register setting

PHY Add.	Register #	Bit	Description	Value
31	5	15	P4EXT	1
31	5	11	MII0_MAC_MODE_EN	0
31	5	10	RMII_EN	0

3.1.5. MII0 SNI MAC mode



● Pin connection



● Pin setting

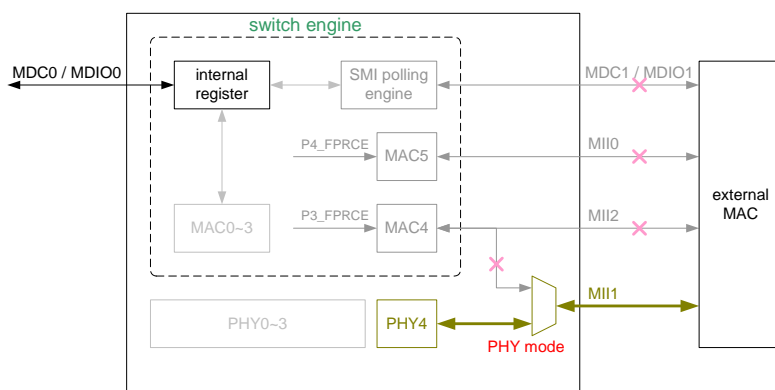
Pin name	setting
P4EXT	1
RMII_EN	0
MII0_MAC_MOD	1
P4MII_SNI	1

● Register setting

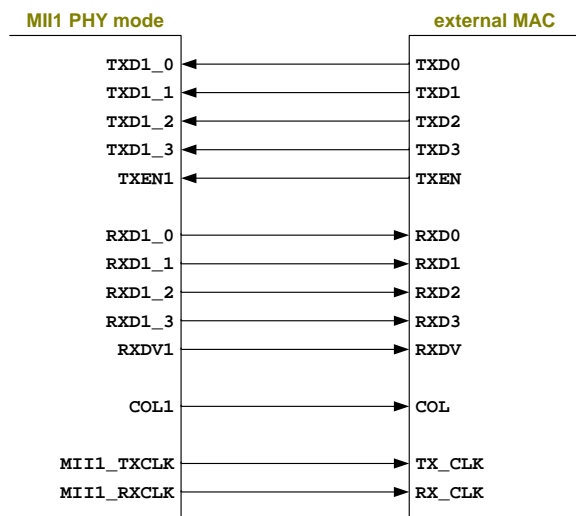
PHY Add.	Register #	Bit	Description	Value
31	3	12:8	Capability of external PHY on MII0	UD
31	3	4:0	MII0_MAC_PHY_ADDR	UD
31	5	15	P4EXT	1
31	5	11	MII0_MAC_MODE_EN	1
31	5	10	RMII_EN	0

3.2. MII1 port⁷

3.2.1. MII1 PHY mode



● Pin connection



● Pin setting

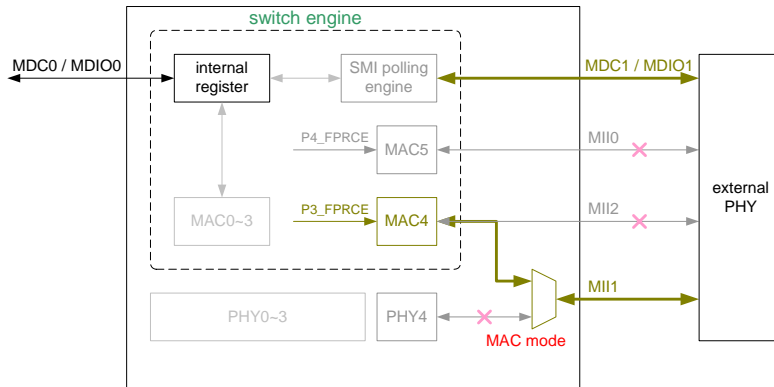
Pin name	setting
P4EXT	1
MII1_DIS	0
MII1_PHY_MOD	1

● Register setting

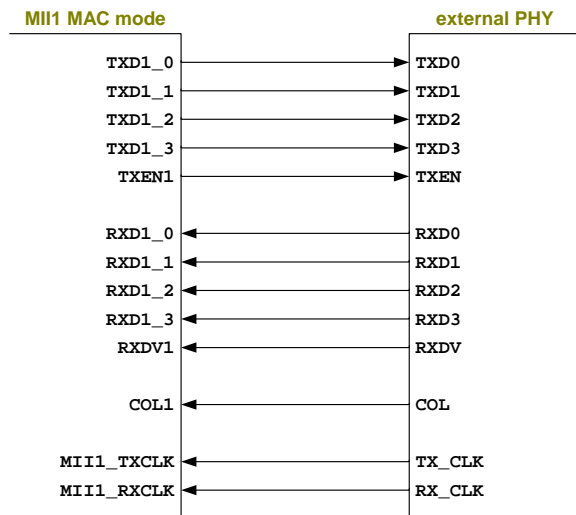
PHY Add.	Register #	Bit	Description	Value
31	5	15	P4EXT	1
31	5	12	MII1_PHY_MODE_EN	1
31	5	10	RMII_EN	0
31	5	8	PHY4_RMII_EN	0

⁷ For prevent the packet is dead locked in the MII0 port, when MII1 port actives, the MII0 port should be configured to PHY mode.

3.2.2. MII1 MAC mode



● Pin connection



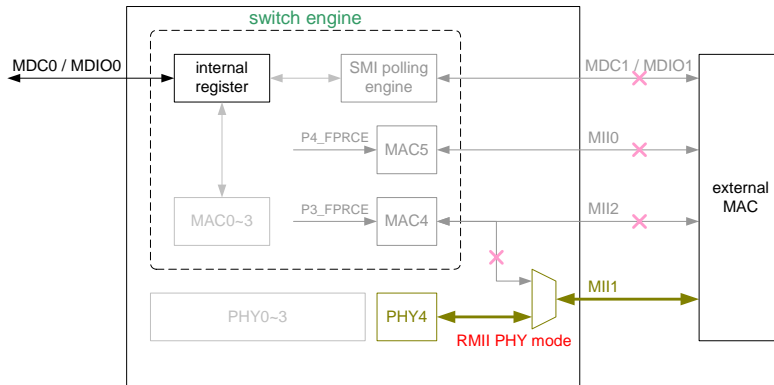
● Pin setting

Pin name	setting
P4EXT	1
MII1_DIS	0
MII2_EN	0
MII1_PHY_MOD	0

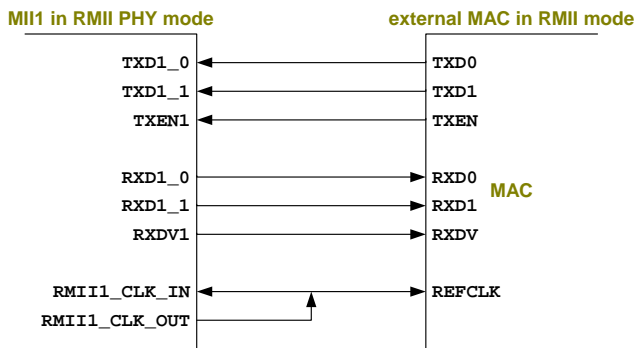
● Register setting

PHY Add.	Register #	Bit	Description	Value
31	4	12:8	Capability of external PHY on MII1	UD
31	4	4:0	MII1_MAC_PHY_ADDR	UD
31	5	15	P4EXT	1
31	5	12	MII1_PHY_MODE_EN	0
31	5	10	RMII_EN	0
31	5	8	PHY4_RMII_EN	0

3.2.3. MII1 RMII PHY mode



● Pin connection



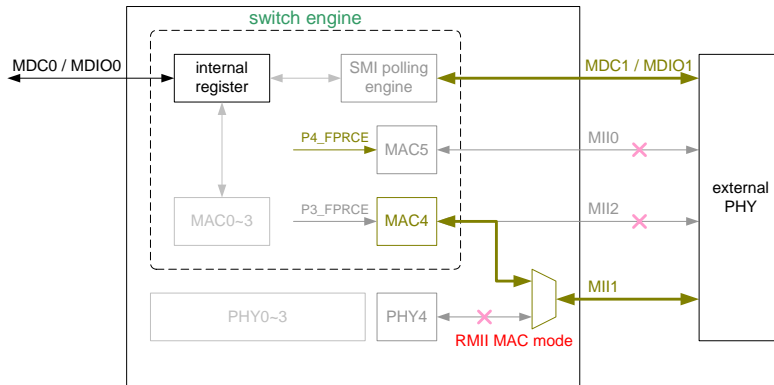
● Pin setting

Pin name	setting
P4EXT	1
MII1_DIS	0
RMII_EN	1
MII1_PHY_MOD	1

● Register setting

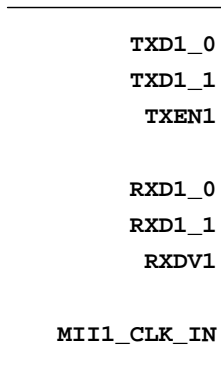
PHY Add.	Register #	Bit	Description	Value
31	5	15	P4EXT	1
31	5	12	MII1_PHY_MODE_EN	1
31	5	10	RMII_EN	1
31	5	8	PHY4_RMII_EN	1

3.2.4. MII1 RMII MAC mode

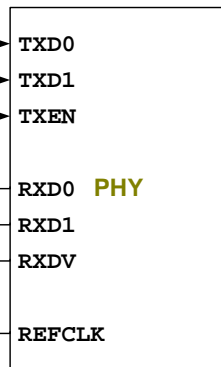


● Pin connection

MII1 in RMII MAC mode



external PHY in RMII mode



● Pin setting

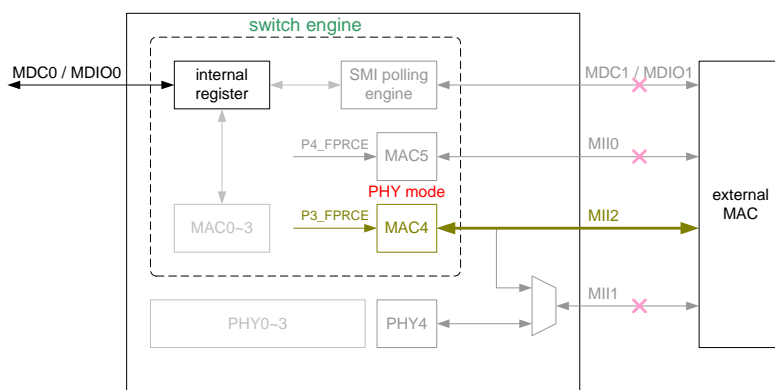
Pin name	setting
P4EXT	1
MII1_DIS	0
MII2_EN	0
RMII_EN	1
MII1_PHY_MOD	0

● Register setting

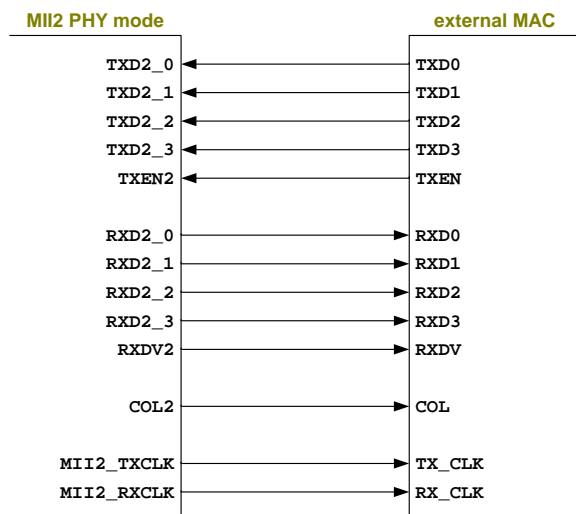
PHY Add.	Register #	Bit	Description	Value
31	4	12:8	Capability of external PHY on MI1	UD
31	4	4:0	MII1_MAC_PHY_ADDR	UD
31	5	15	P4EXT	1
31	5	12	MII1_PHY_MODE_EN	0
31	5	10	RMII_EN	1
31	5	8	PHY4_RMII_EN	1

3.3. MII2 port⁸

3.3.1. MII2 PHY mode



● Pin connection



● Pin setting

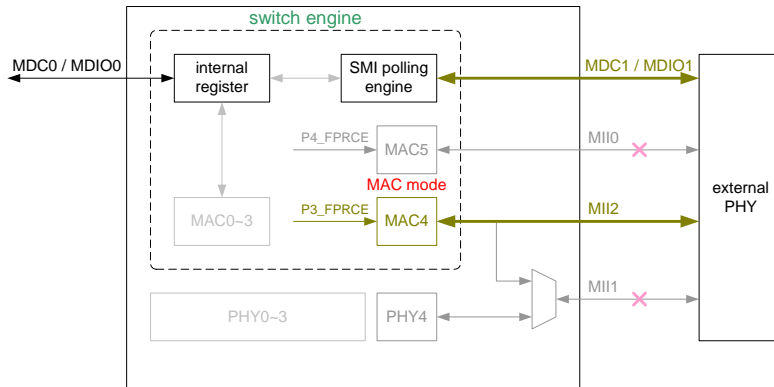
Pin name	setting
P4EXT	1
MII2_EN	1
RMII_EN	0
MII2_MAC_MOD	0

● Register setting

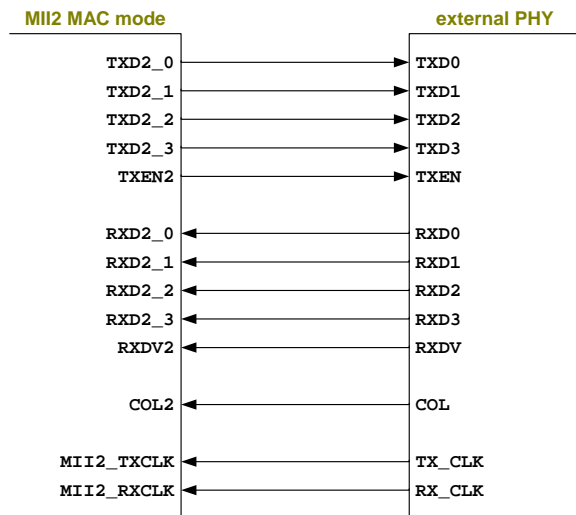
PHY Add.	Register #	Bit	Description	Value
31	5	15	P4EXT	1
31	5	10	RMII_EN	0
31	5	2	MII2_EN	1
31	5	0	MII2_MAC_MOD	0

⁸ The MII2 port and the indication LEDs are use the same pin location, so when MII2 port are in using, the LEDs should be configured to serial mode.

3.3.2. MII2 MAC mode



● Pin connection



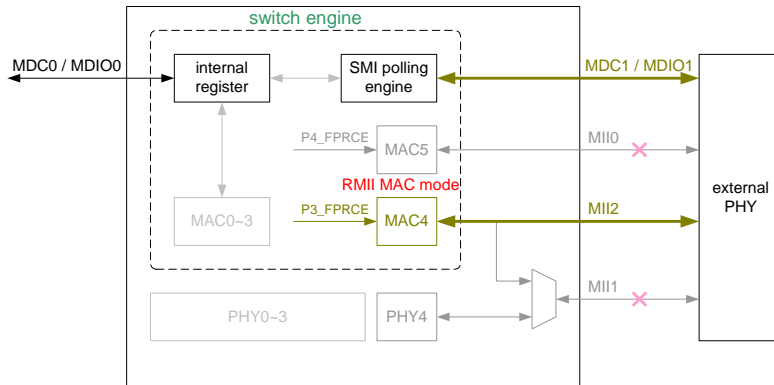
● Pin setting

Pin name	setting
P4EXT	1
MII2_EN	1
RMII_EN	0
MII2_MAC_MOD	1

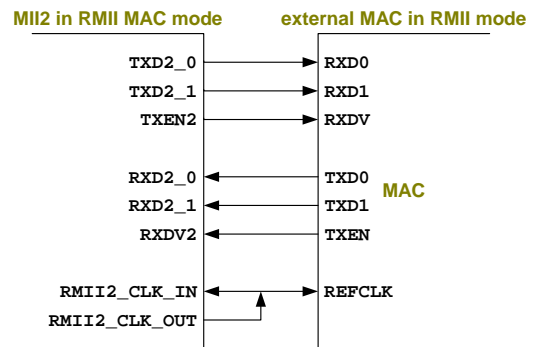
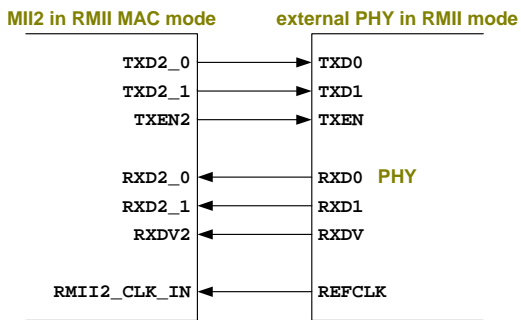
● Register setting

PHY Add.	Register #	Bit	Description	Value
31	4	12:8	Capability of external PHY on MII1	UD
31	4	4:0	MII1_MAC_PHY_ADDR	UD
31	5	15	P4EXT	1
31	5	10	RMII_EN	0
31	5	2	MII2_EN	1
31	5	0	MII2_MAC_MOD	1

3.3.3. MII2 RMII MAC mode



● Pin connection⁹



● Pin setting

Pin name	setting
P4EXT	1
MII2_EN	1
RMII_EN	1
MII2_MAC_MOD	1

● Register setting

PHY Add.	Register #	Bit	Description	Value
31	4	12:8	Capability of external PHY on MII1	UD
31	4	4:0	MII1_MAC_PHY_ADDR	UD
31	5	15	P4EXT	1
31	5	10	RMII_EN	1
31	5	2	MII2_EN	1
31	5	0	MII2_MAC_MOD	1
31	5	10	RMII_EN	1

⁹ Under this mode, this port can be connected to an external PHY or MAC device.